

Quentin J. Lewis

Summary

- A self-starting problem solver who likes to get things done. Has extensive hardware development experience working for fast paced, industry-leading computer companies.
- Understands the big picture, and works well in cross-functional teams to produce the best product design. Experience organizing a department/teams work process that create results that are high quality, consistent, and conform to industry “best-practices”.
- Extensive experience managing internal and outsourced project teams: keeping milestones, objectives and decisions synchronized between all participants.
- Experience in staffing, training, mentoring and evaluating personnel to maximize productivity, maintain good employee moral, maintaining end-goal focus and ensure that standards for quality output are understood and strived for.
- Extensive hand-on experience with high-speed system/board designs; including both microprocessor and I/O subsystem boards. Worked with Orcad Capture, Allegro Layout, and a variety of signal integrity simulation packages. Designs included work with SPARC, Intel x86, AMD K6 CPUs, Microchip micro-controllers, Solaris OS, DOS, Win9x, Win2K, and WinXP operating systems.

Work experience

Sun Microsystems Inc., Burlington, Ma.

Nov. 2004 – Present

MTS, Sustaining Engineering, WGS (*Workgroup Servers*)

- Perform sustaining Engineering functions in support of Sunfire 880/890 and Sunfire 480/490 product lines.
- Productize product enhancements, fixes and speed bumps.

Kentron Technologies Inc., Wilmington, Ma.

Dec 2000 – Mar 2004

Director of Engineering

- Reported to President/CTO and CEO
- Organized and headed Engineering Department
 - Directed and worked with three Development Engineers and one Technician.
 - Oversaw new product development, sustaining engineering, and field and sales support
 - Linked Engineering, Operations, Sales and Marketing
 - Created standard Product life cycle “Phases” to better communicate. Phases include “Conception, Design Completion, DVT Completed/Released to production, End of Life (EOL)”. Product life process includes sign-off of various departments before product moves between phases to better manage product transitions across the whole company.
 - Developed and normalized a process for product development, Design Verification Testing (DVT) and product hand-off to production. Created company wide review and “sign-off” process for ECO change and product release.
 - Instituted enhanced DVT test procedure for new product designs going to production. (*included configuration testing across boards, DRAM manufacturers as well as temperature, frequency and voltage margining*)
 - Organized lab and created standard “testbed” set-ups to simplify test set-up and minimize test disruptions.
 - Cataloged lab test software and test suites into standard form and made them available across the network via a server to simplify disaster recovery, and minimize general testing set-up time.
 - Performed Schematic capture of all DIMM designs using Cadence Orcad Capture. Performed

PCB layout reviews using both Cadence Allegro and several freeware Gerber Viewers.

- Headed development of QBM products
 - Created QBM “design guide” that organized overall QBM technical information so that chip designers (*like ICS, ST Microelectronics and VIA*), board/system designers could implement QBM in their product designs.
 - Conceived of and wrote a specification for a QBM clock generator. Worked with ICS Engineers who designed the device, and then performed device timing characterization and DVT on the ICS8781 QBM clock generator (*on the bench and in application*)
 - Wrote a specification for the QBM10R FET switch device that was the heart of QBM. Worked with ST Microelectronics to help them understand the important timing parameters. Performed device timing characterization and DVT of the final FET devices. (*and the several revisions of the FET switches*) Worked with VIA Technologies to design a QBM interface into their PT880 chipset. Debugged QBM interface in the PT880 based board both at Kentron and at VIA in Taiwan.
- Headed efforts to electrically characterize and develop FEMMA technology products
 - Headed team creating high performance, high density, “first in class” products using FEMMA
 - Created spice models for FEMMA flex circuits using TDR and TDA systems Iconnect Software
 - Worked with IBM to analyze how FEMMA would benefit not only their products requiring standard JEDEC DIMMs, but some of their proprietary DIMM designs as well.
 - Performed thermal characterization measurements of FEMMA vs stacking, and created reports showing the FEMMA advantage
 - Worked to create a better heat spreading technique that would allow the even tighter folding of FEMMA boards. (*better cooling*)
 - Performed a number of experiments and wrote various reports that were presented at JEDEC in attempts to make FEMMA a JEDEC standard.

Sun Microsystems Inc., Burlington, Ma.

Dec. 1987 – Dec 2000

MTS-5, Program Manager, Hardware Lead SunPCi-II (*Penguin II*)

- Chairman of the SunPCi Business Team meetings (*Ops, Marketing, Engineering, Field Service*)
- Coordinated Engineering effort (*schedule, resources*)
- Managed ODM partner’s product hardware development (*Mitac International Corp. in Taiwan*)

MTS-5, Hardware Project Lead, SunPCi (*Penguin*)

Communications liaison between Mitac in Taiwan, and Sun Engineering on this PC compatible card with a 300MHz K6-2 processor that allows people using Sun workstations to run Windows 9x, and Windows NT (*and their applications*) native.

Coordinated various west coast Sun groups (*Agency, Mechanical*) when they worked with Mitac solving SunPCi problems.

Performed Low level prototype bring-up/debug

MTS-5, Technical Lead, Enterprise 450 (*Tazmo*)

- Led design team doing quad 300MHz UltraSPARC II Processor SparcServer 450 Enterprise Server development. Led team making all technical design decisions, and creating final design.
- Planned and oversaw all lab debug efforts and activity.

MTS-5, Technical Lead, (*Positron – program cancelled*)

- Board designer on Positron system development. (*Positron was Sun Microsystems first PCI system, eventually canceled and produced only as a Sun-PCI development platform*)
- Designed motherboard and PCI riser with single 200MHz UltraSPARC I processor and three PCI slots with one slot being a PCI-66 slot.
- Coordinated all engineering disciplines as technical lead and owner of the Engineering team.
- Organized daily lab-debug activities and directed ECO writers submitting change orders.

MTS-4, System Board Designer, SPARCstation LX/Classis (*Sunergy*)

- Designed boards and performed/coordinated board debug on SparcStation LX and SparcCLASSIC systems. Performed all schematic capture with Cadence Concept and performed timing simulation with Quad Design TLC.

MTS-3, Hardware Lead/Board Design, Sun 486I (*Apache – program cancelled*)

- Lead engineer of group creating next generation 386I product.
- Created Processor on Plug-in (*POP*) architecture for simplified upgrade and "mid-life" kickers as 486 clock rate increases came about.
- Worked with Intel to perform very large UNIX address traces and wrote 486 cache simulator in C to help "tune" the POP architecture and the cache sizes of the various POP modules.

MTS-3, Design Engineer, Sun 386I (*Roadrunner*)

- Came to Sun to "get the 386I out the door" and into production.
- Performed much system I/O benchmarking and analysis for future use in 486i architecture analysis.

Prior
Employment

Apollo Computer Inc., Chelmsford, Ma.

Rixon Inc., Silver Spring, Md.

Instrumentation Labs Inc., Lexington, Ma.

Education

2004 Northern Essex Community College Haverhill, Ma

Continuing Education Certificate/Entrepreneurial Training Program

20-Week intensive program covering aspects of starting, running and growing a new business, including the creation of a complete and well thought out business plan.

1977 – 1980 Wentworth Institute of Technology Boston, Ma

BSET/Electrical Engineering Technology

Graduated Cum Laude 1980 (Cumulative Average – 3.56/4.00), Presidents List and Deans List, Member of Tau Alpha Pi Fraternity

AS/Engineering with studies in Electronics Technology

Graduated Cum Laude 1978 (Cumulative Average – 3.65/4.00), Presidents List and Deans List

Patents and
publications

US Patent #5,706,173 – Support for long PCI card in computer enclosure

US Patent #5,906,315 – Watchdog timer for controlling a cooling system

US Patent #6,289,467 – Installation of processor and power supply modules in a multiprocessor system

US Patent #6,349,353 - System and method for detecting and routing between an optional plug-in controller and multiple fixed peripheral backplanes

US Patent #6,567,877 - Automatically enabling terminator for internal SCSI buses with external SCSI bus expansion

Community
activities

Elected Aaron Cutler Memorial Library Trustee (*1995-2004*)

Elected Litchfield Budget Committee (*1990-1993*)

Litchfield School Technology Committee volunteer. (Work on Technology plan. Prepared budgets requests for town meetings. Chairman of the teacher Training and Extracurricular Teacher Support Committees. Set-up and install hardware and software.)

Red Cross Disaster Team Volunteer. First Aid/CPR/AED Certified

Parent Volunteer on Presentation of Mary Academy Parent Group Computer Committee (Volunteer coordination, classroom and lab networking, PC hardware/software installation, teacher training, fundraising)

Organizer & Volunteer on USFirst Teams at Alvirne (*2000*) and Bishop Guertin High School (*2002,2003&2004*) Teams. Team lead for the Bishop Guertin 2003&2004 USFirst team. The 2003 Team was a Granite State Regional Johnson and Johnson Sportsmanship Award Winner, and Nationals Quarterfinalist participant. The 2004 Team was the Granite State Regional Chairman's Award Winner.

